40Gb/s QSFP+ Parallel Active Optical Cable (AOC)

QSFP-40G-XXAOC

Product Specification

Features

- 4 independent full-duplex channels
- Up to 11.2Gb/s data rate per channel
- QSFP+ MSA compliant
- Up to 100m transmission
- Operating case temperature: 0~70°C
- Single 3.3V power supply
- Maximum power consumption 1.5W each terminal
- RoHS-6 compliant

Applications

- 10/40G Ethernet
- Infiniband SDR/DDR/QDR
- 2/4/8G Fiber Channel

Part Number Ordering Information

QSFP-40G-xxAOC	QSFP+ active optical cable with full real-time digital diagnostic monitoring

where "xx" denotes cable length in meters. Examples of cable length offered are as follows:

xx = 01 for 1m	xx = 50 for 50m
xx = 05 for 5m	xx = 75 for 75m
xx = 10 for 10m	xx = 00 for 100m

1. General Description

This product is a high data rate parallel active optical cable (AOC), to overcome the bandwidth limitation of traditional copper cable. The AOC offers 4 independent data transmission channels and 4 data receiving channels via the multimode ribbon fibers, each capable of 10Gb/s operation. Consequently, an aggregate data rate of 40Gb/s over 100 meters transmission can be achieved by this product, to support the ultra-fast computing data exchange.

The product is designed with form factor, optical/electrical connection according to the QSFP+ Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

2. Functional Description

This product converts the parallel electrical input signals into parallel optical signals (light), by a driven Vertical Cavity Surface Emitting Laser (VCSEL) array. The light propagates through the ribbon fiber individually, and be captured by the photo diode array. The optical signals are converted into parallel electrical signals and outputted. Consequently, each terminal of the cable has 8 ports, 4 for data transmission and 4 for data receiving, to provide totally 40Gb/s data exchange. Figure 1 shows the functional block diagram of the parallel AOC.

A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP+ memory map.

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of

reset interrupt without requiring a reset.

Low Power Mode (LPMode) pin is used to set the maximum power consumption for the product in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground though a resistor on the host board and asserts the signal. ModPrsL then indicates it is present by setting ModPrsL to a "Low" state.

Interrupt (IntL) is an output pin. "Low" indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

3. AOC Block Diagram

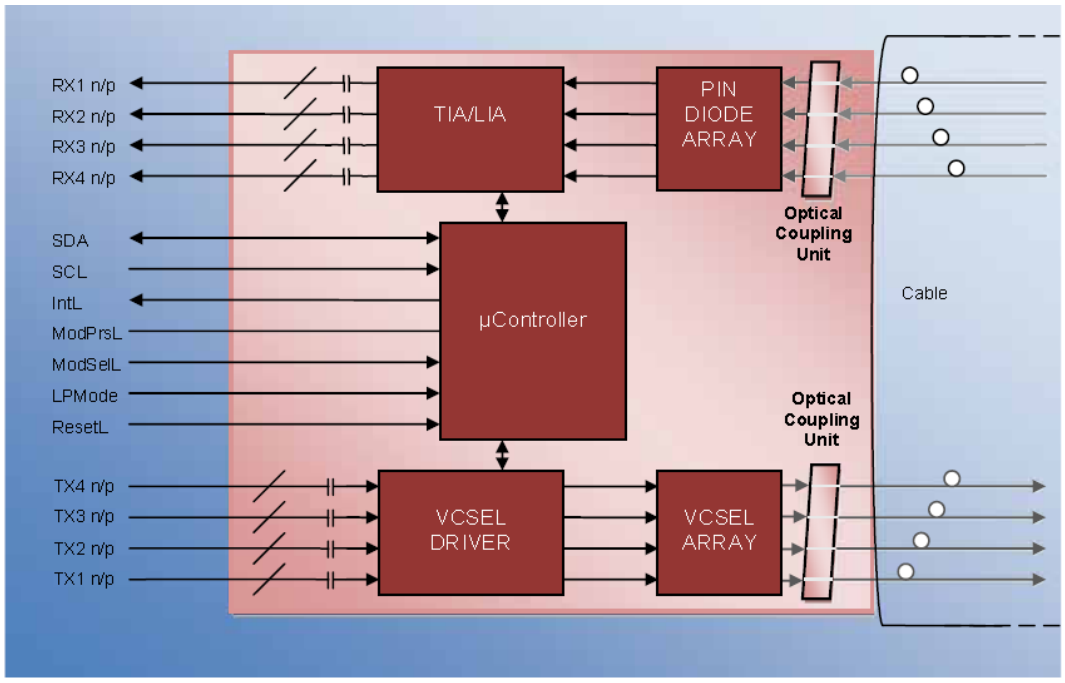

Figure 1. Block Diagram of One of the QSFP+ End Modules

4. Pin Assignment and Pin Description

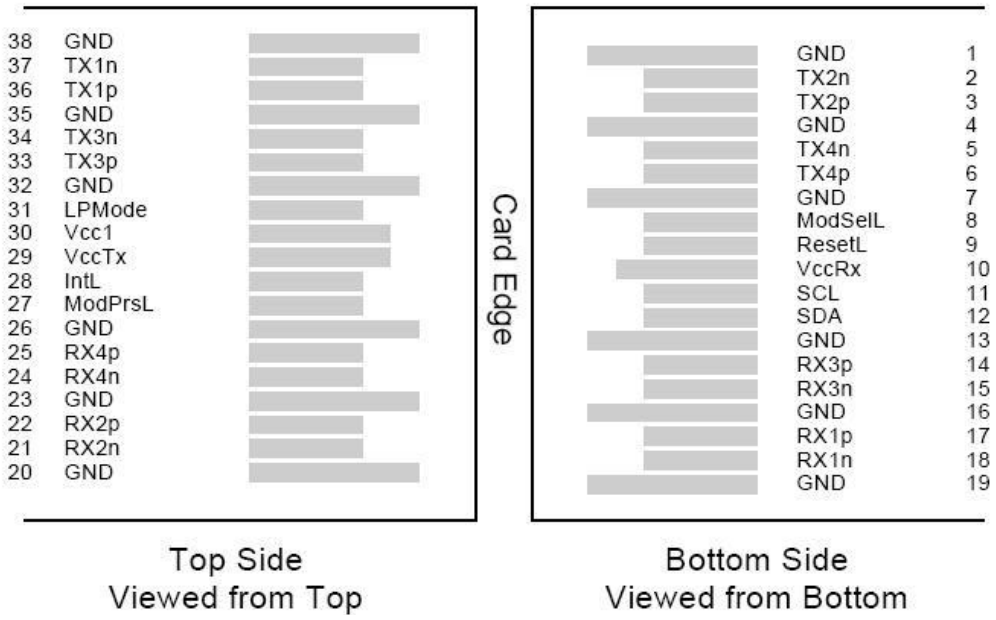

Figure 2. MSA compliant Connector

5. Pin Definition

PIN	Logic	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	

15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

Notes:

1. GND is the symbol for signal and supply (power) common for QSFP+ modules. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure 3 below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP+ transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

6. Recommended Power Supply Filter

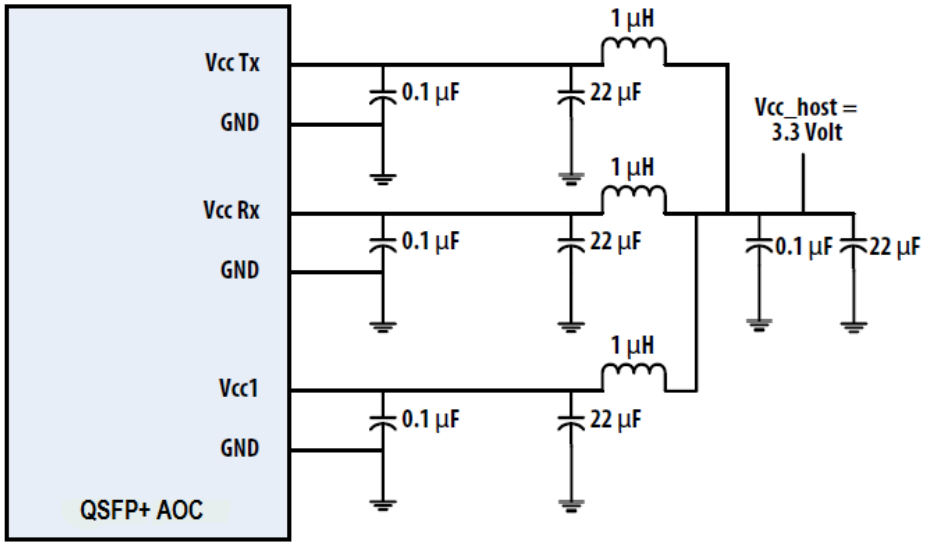

Figure 3. Recommended Power Supply Filter

7. Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	T_S	-40	85	degC	
Operating Case Temperature	T_{OP}	0	70	degC	
Power Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	

8. Recommended Operating Conditions and Power Supply Requirements

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	T_{OP}	0		70	degC
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Data Rate, each Lane			10.3125	11.2	Gb/s
Control Input Voltage High		2		Vcc	V
Control Input Voltage Low		0		0.8	V

9. Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating temperature and supply voltage unless otherwise specified.

Parameter	Symbol	Min.	Typical	Max	Unit	Notes
Power Consumption, each Terminal				1.5	W	
Supply Current, each Terminal	Icc			450	mA	
Transceiver Power-on Initialization Time				2000	ms	
Transmitter (each Lane)						
AC Common Mode Input Voltage Tolerance (RMS)		15			mV	
Differential Input Voltage Swing Threshold		50			mVpp	LOSA Threshold
Differential Input Voltage Swing	Vin,pp	180		1200	mVpp	
Differential Input Impedance	Zin	90	100	110	Ohm	
Differential Input S-parameter	SDD11	< -12 + 2 × SQRT(f), with f in GHz.			dB	0.01-4.1GHz
		< -6.3 + 13 × log10(f/5.5), with f in GHz			dB	4.1-11.1GHz
Reflected Differential to Common Mode Conversion	SCD11			-10	dB	0.01-11.1GHz
Total Jitter				0.40	UI	
Deterministic Jitter				0.15	UI	
Receiver (each Lane)						
AC Common Mode Output Voltage (RMS)				7.5	mV	
Differential Output Voltage Swing	Vout,pp	600		800	mVpp	

Differential Output Impedance	Zout	90	100	110	Ohm	
Differential Output S-parameter	SDD22	< -12 + 2 × SQRT(f), with f in GHz			dB	0.01-4.1GHz
		< -6.3 + 13 × log10(f/5.5), with f in GHz			dB	4.1-11.1GHz
Common Mode Output Reflection Coefficient	SCC22	< -7 + 1.6 × f, with f in GHz.			dB	0.01-2.5GHz
				-3	dB	2.5-11.1GHz
Total Jitter				0.38	UI	In the case the specs of Tx jitters are met
Deterministic Jitter				0.64	UI	

10. Mechanical Dimensions

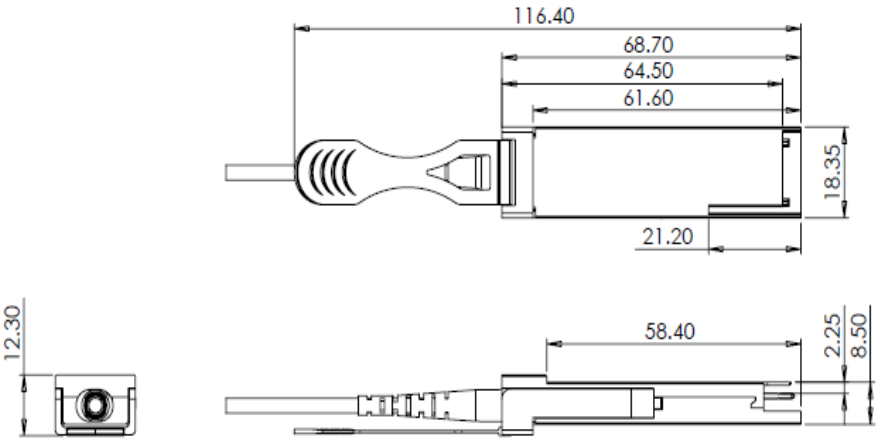

Figure 4. Mechanical Outline

11. ESD

This transceiver is specified as ESD threshold 1kV for SFI pin and 2kV for all others electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.